Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claim 1 (Currently Amended): A semiconductor device comprising:

a substrate having an insulating layer formed thereon;

a silicon layer having a thickness ts formed on the insulating layer, the silicon layer including a first area having a first impurity concentration of Df cm^{-3}, and a second area having a second impurity concentration ~~condition~~ of Dp cm^{-3};

a fully-depleted MOSFET formed in the first area of the silicon layer ~~substrate~~; and

a partially-depleted MOSFET formed in the second area of the silicon layer[[;]],

wherein the semiconductor device satisfies the following conditions ~~condition~~:

$28\ nm \leq ts \leq 42\ nm$,

$Df \leq 9.29 * 10^{15} * (62.46 - ts)$,

$Df \leq 2.64 * 10^{15} * (128.35 - ts)$,

$Dp \geq 9.29 * 10^{15} * (62.46 - ts)$, and

$Dp \geq 2.64 * 10^{15} * (129.78 - ts)$.

Claim 2 (Currently Amended): A semiconductor device according to claim 1, wherein the device satisfies a condition of $Df \leq 3.00 * 10^{15} * (102.67 - ts)$.

Claim 3 (Currently Amended): A semiconductor device according to claim 1, wherein the device satisfies a condition of $Dp \geq 3.29 * 10^{15} * (125.70 - ts)$.

Claim 4 (Currently Amended): A semiconductor device according to claim 1, wherein the thickness of the silicon layer has a range of 38 nm to 42 nm, the first impurity concentration Df is equal to or more than $1.9 * 10^{17}$ cm^{-3}, and the second impurity concentration Dp is equal to or less than $2.2 * 10^{17}$ cm^{-3}.

Claim 5 (Currently Amended): A semiconductor device according to claim 1, wherein the thickness of the silicon layer has a range of 33 nm to 37 nm, the first impurity concentration [[of]] Df is equal to or less than $2.5 * 10^{17}$ cm^{-3}, and the second impurity concentration Dp is equal to or more than $2.7 * 10^{17}$ cm^{-3}.

Claim 6 (Currently Amended): A semiconductor device according to claim 1, wherein the thickness of the silicon layer has a range of 28 nm to 32 nm, the first impurity concentration [[of]] Df is equal to or less than $2.7 * 10^{17}$ cm^{-3}, and the second impurity concentration Dp is equal to or more than $3.2 * 10^{17}$ cm^{-3}.

Claim 7 (New): A semiconductor device comprising:

a silicon substrate;

a buried oxide layer formed on the silicon substrate;

an SOI layer formed on the buried oxide layer, the SOI layer having a thickness ts of about 28nm to 42nm, the SOI layer having a fully-depleted area having a first impurity concentration Df (cm^{-3}) and a partially-depleted area having a second impurity concentration Dp (cm^{-3});

a first MOS transistor formed on the fully-depleted area of the SOI layer; and

a second MOS transistor formed on the partially-depleted area of the SOI layer,

wherein the first and second impurity concentrations satisfy the following conditions:

$Df \leq 9.29 * 10^{15} * (62.46 - ts)$,

$Df \leq 2.64 * 10^{15} * (128.35 - ts)$,

$Dp \geq 9.29 * 10^{15} * (62.46 - ts)$, and

$Dp \geq 2.64 * 10^{15} * (129.78 - ts)$.

Claim 8 (New): A semiconductor device according to claim 7, wherein the first impurity concentration satisfies a condition of $Df \leq 3.00 * 10^{15} * (102.67 - ts)$.

Claim 9 (New): A semiconductor device according to claim 7, wherein the second impurity concentration satisfies a condition of $Dp \geq 3.29 * 10^{15} * (125.70 - ts)$.

Claim 10 (New): A semiconductor device according to claim 7, wherein the thickness ts is about 38 nm to 42 nm, the first impurity concentration Df is equal to or more than 1.9 * 10^{17} cm^{-3}, and the second impurity concentration Dp is equal to or less than 2.2 * 10^{17} cm^{-3}.

Claim 11 (New): A semiconductor device according to claim 7, wherein the thickness ts is about 33 nm to 37 nm, the first impurity concentration Df is equal to or more than 2.5 * 10^{17} cm^{-3}, and the second impurity concentration Dp is equal to or less than 2.7 * 10^{17} cm^{-3}.

Claim 12 (New): A semiconductor device according to claim 7, wherein the thickness ts is about 28 nm to 32 nm, the first impurity concentration Df is equal to or more than 2.7 * 10^{17} cm^{-3}, and the second impurity concentration Dp is equal to or less than 3.2 * 10^{17} cm^{-3}.

Claim 13 (New): A semiconductor device comprising:

a semiconductor substrate;

a buried oxide layer formed on the substrate;

a silicon layer formed on the buried oxide layer, the silicon layer having a thickness ts of about 28 nm to 42nm, the silicon layer having a fully-depleted area having a first impurity concentration Df (cm^{-3}) and a partially-depleted area having a

second impurity concentration Df (cm^{-3});

a first source and a first drain formed on the fully-depleted area of the silicon layer;

a first gate insulating layer formed on the fully-depleted area of the silicon layer between the first source and the first drain;

a first gate electrode formed on the first gate insulating layer;

a second source and a second drain formed on the partially-depleted area of the silicon layer;

a second gate insulating layer formed on the partially-depleted area of the silicon layer between the second source and the second drain; and

a second gate electrode formed on the second gate insulating layer,

wherein the first and second impurity concentrations satisfy the following conditions:

$Df \leq 9.29 * 10^{15} * (62.46 - ts)$,

$Df \leq 2.64 * 10^{15} * (128.35 - ts)$,

$Dp \geq 9.29 * 10^{15} * (62.46 - ts)$, and

$Dp \geq 2.64 * 10^{15} * (129.78 - ts)$.

Claim 14 (New): A semiconductor device according to claim 13, wherein the first impurity concentration satisfies a condition of $Df \leq 3.00 * 10^{15} * (102.67 - ts)$.

Claim 15 (New): A semiconductor device according to claim 13, wherein the second impurity concentration satisfies a condition of $Dp \geq 3.29 * 10^{15} * (125.70 - ts)$.

Claim 16 (New): A semiconductor device according to claim 13, wherein the thickness ts is about 38 nm to 42 nm, the first impurity concentration Df is equal to or more than $1.9 * 10^{17}$ cm^{-3}, and the second impurity concentration Dp is equal to or less than $2.2 * 10^{17}$ cm^{-3}.

Claim 17 (New): A semiconductor device according to claim 13, wherein the thickness ts is about 33 nm to 37 nm, the first impurity concentration Df is equal to or more than $2.5 * 10^{17}$ cm^{-3}, and the second impurity concentration Dp is equal to or less than $2.7 * 10^{17}$ cm^{-3}.

Claim 18 (New): A semiconductor device according to claim 13, wherein the thickness ts is about 28 nm to 32 nm, the first impurity concentration Df is equal to or more than $2.7 * 10^{17}$ cm^{-3}, and the second impurity concentration Dp is equal to or less than $3.2 * 10^{17}$ cm^{-3}.